AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 18, line 16, with the following rewritten paragraph.

--In the above-described embodiment, the link base layer 11, the base 12, and the highly doped selective collector 14 positioned directly under the base are formed by ion implantation by way of the same opening portion; however, various modifications are possible within the scope of the present invention. For example, they may be formed after formation of the side walls 7a for isolating the emitter ~~form~~from the base. Moreover, each diffusion layer may be formed by plasma doping or the like. In addition, the profiles of the emitter, base and collector can be selectively formed in accordance with the kinds of transistors. The profiles of the link base layer and the highly doped collector layer positioned directly under the base can be optimized in accordance with the kinds of the transistors.--

Please replace the paragraphs beginning on page 2, line 5, with the following rewritten paragraph.

--The bipolar transistor having the above-described structure is fabricated in the following procedures. First, as shown in FIG. 4A, an insulating film (SiO_2 film) 2 having a thickness of from 100 to 200 nm is formed over the surface of a silicon substrate 1 by or CVD.

As shown in FIG. 4B, an opening is formed for a base electrode of the bipolar transistor. Reference numeral 2a indicates an opening side wall. A p-type polysilicon (poly-Si) film 3 having a thickness of from 100 to 200 mm is formed over the surface by CVD. The p-type poly-Si film 3 serves as a base electrode. It is to be noted that the doping of a p-type impurity to the poly-Si can be also performed by ion implantation.

Next, as shown in FIG. 4C, an insulating film (SiO_2 film) 4 having a thickness of from 300 to 400 nm is formed over the surface of the wafer by CVD, and then an opening 10 for forming an emitter and a base is formed by dry etching, of the laminated films, the SiO_2 film 4 and the p-type poly-Si film 3. After that, an insulating film (SiO_2 film) 5 having a thickness of from 10 to 20 nm is formed over the surface by CVD, and a p-type impurity

diffusion layer 6 is formed by ion implantation through the SiO_2 film 5. In this case, for example, ions of BF_2 are implanted in a dose of from $1x10^{13}$ to $1x10^{14}$ cm^{-2} at an implantation energy of from 20 to 30 KeV. The p-type impurity diffusion layer 6 serves as the base, and the SiO_2 film 5 having a thickness of from 10 to 20 nm serves as a buffer layer for preventing a channeling tail upon ion implantation for forming the base. The ion implantation is followed by heat-treatment (annealing) for 10 to 20 minutes at 900°C, to form a P^+ contact layer (graft contact) 3a in the silicon substate 1 by diffusion from the p-type poly-Si film 3.

Next, as shown in FIG. 5A, a side wall forming insulating film (SiO_2 film) 7 having a thickness of from 400 to 600 nm is formed over the surface by CVD. The SiO_2 film 7 is then removed by anisotropic etching such as RIE so as to form side walls 7a made of the SiO_2 film in the opening for forming an emitter and a base, as shown in FIG. 5B. The side wall 7a has a function of isolating the base electrode made of the p-type poly-Si film 3 from an emitter electrode which will be formed later.--

Please replace the paragraph beginning on page 16, line 9, with the following rewritten paragraph:

--With the above-described sequential processes, (1) the concentration of the base 12 (including the link base layer 11) at a portion directly under the side wall 7a isolates the emitter from the base without any increase in the base concentration at a portion directly under the emitter, thus preventing variations in characteristics due to variations in a ~~correct~~collector current or the base re-recombination current at such a portion, and ensuring reliability; and (2) an increase in the thickness of the base 12 is suppressed.--